

REMARKS

This Amendment responds to the Office Action dated April 3, 2003 in which the Examiner objected to the claims and drawings, rejected claim 6 under 35 U.S.C. §112, first paragraph, rejected claims 1-4 and 6 under 35 U.S.C. §102(a) rejected claims 7-9 and 13-15 under 35 U.S.C. §103 and objected to claims 5, 10-12 and 16 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

Applicants respectfully traverse the Examiner's objection to the claims. Applicants respectfully bring the Examiner's attention to §608.01(n) of the MPEP which gives various examples for multiple dependent claims. As shown in the Examples, none of the dependent claims starts with the word "The". Furthermore, claim 3 lines 4 and 5 refer to first and second diffused layers. Therefore, Applicants respectfully submit that it would be improper to change the word "layers" to "layer". It is therefore respectfully requested that the Examiner withdraws the objection to the claims.

As indicated above, a minor typographical error in claim 3 has been corrected. It is respectfully requested that the Examiner approves the correction. Applicants respectfully submit that the amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claim.

Applicants respectfully traverse the Examiner's objection to the drawings. Applicants respectfully bring the Examiner's attention to Figure 14 which shows the isolation area 70 as well as first, second and third diffused layers 20, 21 and 22 claimed in claim 6. Furthermore, Applicants respectfully bring the Examiner's attention to Figures 23-28 which shows the source and drain areas opposed to each other across the channel

portion of the substrate as claimed in claims 11 and 12. Therefore, Applicants respectfully request the Examiner withdraws the objection to the drawing under 37 C.F.R. §1.83(a).

Applicants respectfully traverse the Examiner's rejection of claim 6 under 35 U.S.C. §112, first paragraph. Applicants respectfully bring the Examiner's attention to page 14 line 23 through page 15 line 6 as well as to Figure 14. It is respectfully submitted that the specification provides support for claim 6 and that the specification describes the invention in such a way to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 6 under 35 U.S.C. §112, first paragraph.

Claim 1 claims a semiconductor device comprising a gate electrode, first and second diffused layers, a wiring layer and a contact. The gate electrode is formed on a substrate through a gate insulating film lying therebetween. The first and second diffused layers are formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type. Each layer has a second conduction type different from the first conduction type of the substrate portion. The wiring layer is formed above the gate electrode. The contact is formed within a contact hole between the wiring layer and the substrate. The contact electrically connects the wiring layer to the first diffused layer and a side wall of the gate electrode.

Through the structure of the claimed invention having a contact electrically connecting a wiring layer to a) the first diffused layer and b) the side wall of the gate electrode, as claimed in claim 1, the claimed invention provides a semiconductor device

which has an improved soft error resistance. The prior art does not show, teach or suggest a contact electrically connecting a wiring layer to a side wall of the gate electrode as claimed in claim 1.

Claim 4 claims a semiconductor device comprising a gate electrode, a diffused layer, a wiring layer and a contact. The gate electrode is formed on a substrate through a gate insulating film. The diffused layer is formed on the substrate. The wiring layer is formed above the gate electrode. The contact is formed within a contact hole between the wiring layer and substrate. The contact electrically connects the wiring layer to the diffused layers and a side wall of the gate electrode. The diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type. Each of the first and second portions has a second conduction type different from the first conduction type of the portion of the substrate. A third portion connects the first portion to the second portion.

Through the structure of the claimed invention having a contact electrically connecting the wiring layer to both the diffused layer and a side wall of the gate electrode, as claimed in claim 4, the claimed invention provides a semiconductor device with an improved soft error resistance. The prior art does not show, teach or suggest a contact electrically connecting a wiring layer to a side wall of gate electrode as claimed in claim 4.

Claims 1-4 and 6 were rejected under 35 U.S.C. §102(a) as being anticipated by *Igarashi et al.* (U.S. Patent No. 6,190,953). In addition, claims 7, 8, 13 and 14 were rejected under 35 U.S.C. §103 as being unpatentable over *Igarashi et al.*

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(a) and under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allow the claims to issue.

Igarashi et al. appears to disclose as shown in FIG. 3A, a gate insulating film 3 of silicon dioxide having a thickness of about 10 nm and a gate electrode 4 of a polysilicon having a thickness of about 100 nm are stacked on a p-type semiconductor substrate 1. As shown in FIG. 3B, the gate electrode 4 is used as a mask to implant impurities (boron, phosphorus or the like) into the surface of the p-type semiconductor substrate 1 to form diffusion layers 2 serving as sources or drains. By these steps, a MOS transistor is formed. Moreover, an interlayer insulating film 5 of silicon dioxide having a thickness of tens nm is formed so as to cover the whole surface by the CVD method. As shown in FIG. 3C, using the photo-etching, openings 50 and 60 are simultaneously formed by patterning the interlayer insulating film 5. The opening 50 is used for forming a local interconnect LIC, and the opening 60 is used for forming a contact CT. (col. 3, lines 42-59) As shown in FIG. 3D, an electrode material (e.g., tungsten W) 18 is formed on the upper surface of the interlayer insulating film 5 by means of the sputtering so that the openings 50 and 60 are completely filled with the electrode material 18. Thereafter, as shown in FIG. 4A, the etch back of the electrode material 18 is carried out by the CMP method or the like until the upper surface of the interlayer insulating film 5 is exposed. Thus, the electrode material 18 can remain only in the openings 50 and 60. In the opening 50, the gate electrode 4 is electrically connected to the diffusion layer 2, so that a local interconnect LIC is formed. In

the opening 60, a contact CT reaching the diffusion layer 2 is formed. As shown in FIG. 4B, an insulating film 9 of silicon dioxide having a thickness of tens nm is formed on the upper surfaces of the interlayer insulating film 5 and the wiring material 8 by the CVD method. Then, as shown in FIG. 4C, an opening 10 is formed in the insulating film 9 by means of the photo-etching, and as shown in FIG. 4D, a wiring material 11 (e.g., a metal wiring of aluminum) is formed by means of the sputtering to be patterned as shown in FIG. 4E. Thus, a semiconductor device is formed. (col. 3, line 67 through col. 4, line 21)

Thus, *Igarashi et al.* clearly teaches away from the claimed invention and merely discloses an electrode material 18 formed between an insulating film 9 and a diffusion region 2 in region 50. Nowhere in *Igarashi et al.* is it shown, taught or suggested that a contact electrically connects a wiring layer to a sidewall of the gate electrode as claimed in claims 1 and 4. Rather, *Igarashi et al.* clearly teaches away from the claimed invention since, in region 50, the electrode material 18 is formed between an insulating film 9 and the diffusion region 2.

Additionally, *Igarashi et al.* merely discloses that in area 60, the electrode material is formed between a wiring material 11 and the diffusion region 2. Nothing in *Igarashi et al.* shows, teaches, or suggests electrically connecting a wiring layer to a sidewall of gate electrode as claimed in claims 1 and 4. Rather, *Igarashi et al.* merely discloses in area 60 connecting wiring material 11 to diffusion region 2 via material 18.

Since nothing in *Igarashi et al.* shows, teaches or suggests a contact electrically connecting a wiring layer to a sidewall of a gate electrode as claimed in claims 1 and 4, it is

respectfully requested that the Examiner withdraws the rejection to claims 1 and 4 under 35 U.S.C. §102(a).

Claims 2-3, 6-8 and 13-14 depend from claims 1 and 4 and recite additional features. It is respectfully submitted that claims 2-3 and 6 would not have been anticipated by *Igarashi et al.* within the meaning of 35 U.S.C. §102(a) at least for the reasons as set forth above and that claims 7-8 and 13-14 would not have been obvious within the meaning of 35 U.S.C. §103 over *Igarashi et al.* at least for the reasons as set forth above.

Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2-3 and 6 under 35 U.S.C. §102(a) and withdraws the rejection to claims 7-8 and 13-14 under 35 U.S.C. §103.

Claims 9-15 were rejected under 35 U.S.C. §103 as being unpatentable over *Igarashi et al.* in view of *Yaegashi et al.* (U.S. Patent No. 6,472,701).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since *Igarashi et al.* merely discloses an electrode material 18 formed between an insulating film line and a diffusion region 2 in an area 50, nothing in *Igarashi et al.* shows, teaches or suggests a contact electrically connecting a wiring layer to a sidewall of a gate electrode as claimed in claims 1 and 4. Therefore, it is respectfully submitted that since the primary reference of *Igarashi et al.* does not show, teach or suggest the primary feature as claimed in claims 1 and 4, it is respectfully submitted that the

combination of the primary reference with the secondary reference to *Yaegashi et al.* will not overcome the deficiencies of the primary reference. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 9 and 15 under 35 U.S.C. §103.

Since objected to claims 5, 10-12 and 16 depend from allowable claims, it is respectfully requested that the Examiner withdraws the objection thereto.

Thus it now appears that the application is in condition for reconsider and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our
Deposit Account No. 02-4800.

Respectfully submitted,

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